Journal of the Korean Physical Society, Vol. 50, No. 3, March 2007, pp. 885∼888

Transport Spectroscopy of a Quantum Dot in a Silicon-on-Insulator (SOI) MOSFET

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(Received 3 September 2006)

We report transport spectroscopy in a gate-induced quantum dot (QD) based on a silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET). The differential conductance G measurement in the large voltage region shows small conductance peaks, which reveal single-electron tunnelling through exited quantum states of the QD. The discrete energy levels extracted from the differential conductance characteristics agree well with those estimated from a harmonic oscillator approximation. The separation between energy levels is confirmed by using a potential shape extracted from a 3-dimensional device simulation.

PACS numbers: 73.20.D, 85.30.Vw, 85.30.Wx
Keywords: Single-electron transistor, Transport spectroscopy, Energy level, Harmonic oscillator

I. INTRODUCTION

It is well known that the effects of exited quantum states have been observed in a quantum dot (QD) on compound semiconductors at several tens of mK due to the relatively large size of the QD [1,2]. Recent advances in silicon nanofabrication techniques have made it possible to reduce the size of a QD on Si (to below a few ten nm) and to observe transport spectroscopy of Si single-electron transistors (SETs) at higher temperatures [3,4]. However, the exited quantum state in the QD on Si has rarely been studied and has been reported by only a few researchers [3,4].

In this paper, we will report the differential conductance G $(= dI_{ds}/dV_{ds})$ versus the drain voltage V_{ds} in a gate-induced QD based on a silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect-transistor (MOSFET). To investigate the transport spectroscopy of a QD in a SOI MOSFET, we analyze the G-V_{ds} characteristics of two SOI MOSFETs with different size QDs, whose tunnel barriers were induced by two sidewall depletion gates on a Si nanowire fabricated on a separation by implanted oxygen (SIMOX) wafer by means of a sidewall patterning method [5–7], will be analyzed. Discrete energy levels are extracted from the differential conductance characteristics, and they are compared with those calculated from a parabolic confining potential well (harmonic oscillator approximation) approximated from the potential shape simulated by a 3-dimensional (3-D) device simulator.

II. DEVICE STRUCTURE AND EXPERIMENTAL RESULTS

The devices are an SET with sidewall depletion gates on an SOI nanowire fabricated on a SIMOX wafer by

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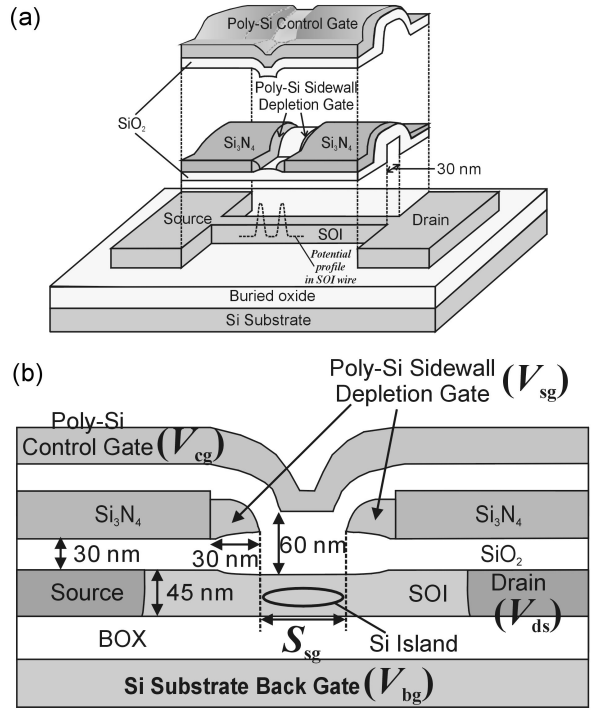

Fig. 1. Schematics of (a) the SET with sidewall depletion gates on a SOI nanowire and (b) its cross-section. Two poly-Si sidewall depletion gates are formed in the edge of the nitride groove. The width of the sidewall gate is 30 nm.

means of a *sidewall patterning* method. We have previously reported that a very uniform lightly p-doped SOI nanowire defined by this patterning method effectively suppressed the unintentional tunnel junctions formed by fluctuations of the geometry or the impurity potential in the SOI wire and that the gate-induced Si dot size dependence of the device characteristics confirmed the good controllability [5, 6]. Figs. 1(a) and 1(b) show a schematic diagram of the fabricated device and its cross-section. The width and the height of the SOI wire are 30 nm and 45 nm, respectively, and the thickness of the control gate oxide is 60 nm. Device operation is as follows: The inversion layer in an SOI wire is created by the back gate voltage, V_{bg}, and two tunnel barriers are formed by the sidewall depletion gate voltage, V_{sg}. The potential of the Si QD in the inversion layer is controlled by using the top control gate voltage, V_{cg}. Therefore, the effective size of a Si dot is determined by the separation between the two sidewall depletion gates (S_{sg} = 90, 140 nm) and the width of the SOI wire (W_{ch} = 30 nm). The details of the fabrication method are given in our previous paper [5,6], and its main feature is that all critical dimensions depend not on the limit of lithography but on the controllability of the conventional Si process technology. Figs. 2(a) and 2(b) show the scanning electron microscopy (SEM) images of the cross-sections of fabricated devices having different S_{sg}'s, 90 nm and 140 nm, respectively.

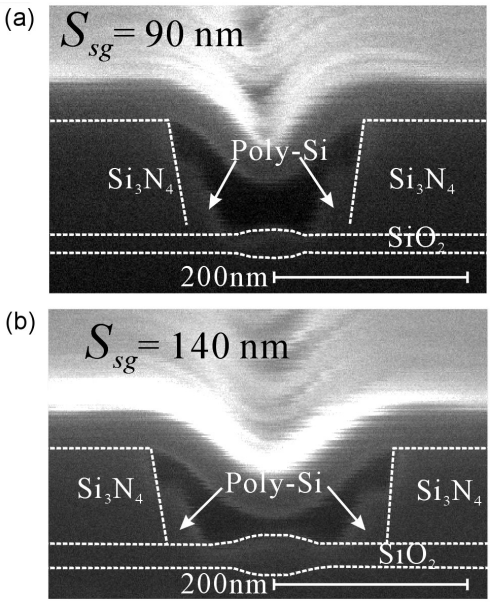

Fig. 2. SEM images of the cross-section of the fabricated Si SETs having a separation between the two sidewall gates of (a) S_{sg} = 90 nm and (b) S_{sg} = 140 nm.

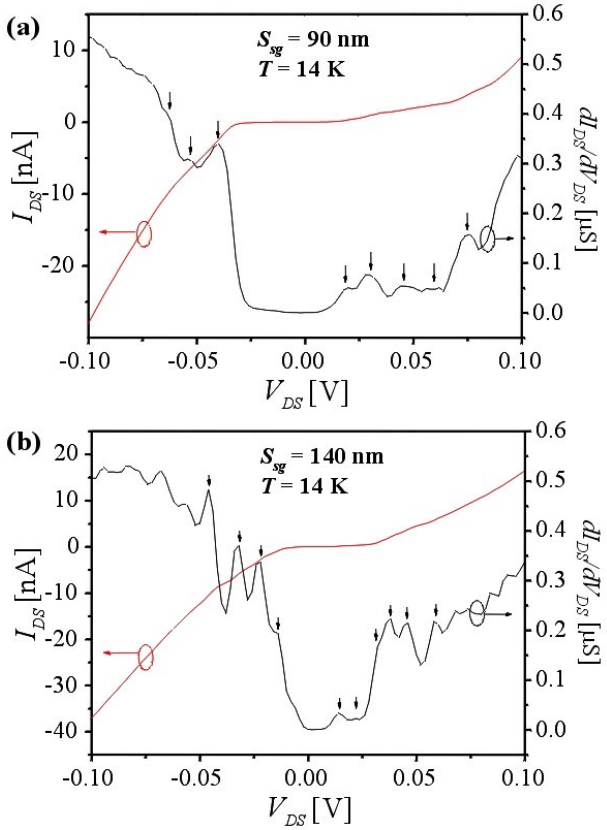

Fig. 3. Differential conductance G of the SET as a function of V_{ds}: (a) S_{sg} = 90 nm and T = 14 K and (b) S_{sg} = 140 nm and T = 14 K. A series of peaks in G are clearly observed, as marked by arrows.

Figs. 3(a) and 3(b) show the differential conductance

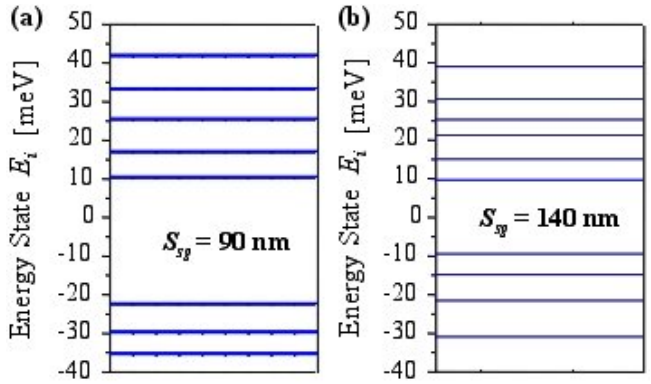

Fig. 4. Experimental excitation spectrum of a QD extracted directly from the data of Fig. 3, with an appropriate scaling of voltage to energy: (a) S_{sg} = 90 nm and T = 14 K and (b) S_{sg} = 140 nm and T = 14 K. Note the two characteristic energy scales, the Coulomb gap and the discrete level spacing.

$G = dI_{ds}/dV_{ds}$ as a function of V_{ds} of SETs with sidewall depletion gates on an SOI nanowire. In these G-V_{ds} curves, at the edge of the Coulomb gap, the large peak in G on either side marks the threshold above which electrons can tunnel into the dot. Beyond these initial peaks in $G(V_{ds})$, a series of additional peaks is seen. The spacing between the peaks is smaller than the Coulomb gap, so it is unexplainable in terms of classical Coulomb blockade theory [8].

III. TRANSPORT SPECTROSCOPY

With the understanding in Section II in hand, it is clear that the peaks and the negative valleys in G correspond to discrete energy levels in the dot. Therefore, a measurement of G can be exploited to map the excitation spectrum, or single-particle states, in a QD [9]. The positions of the differential conductance peaks in V_{ds} have been converted to an energy scale by multiplying V_{ds} by a term, $1 - C_d/C_{total}$, where C_d and C_{total} are the capacitance between the dot and the drain-electrode and the total capacitance in the dot, respectively [8,9]. This accounts for the fact that the potential in the QD partially follows the potential in the biased electrode due to the finite capacitance C_d. Carrying out this procedure on the data in Fig. 3 gives the spectrum shown in Fig. 4. In the case of the SET with S_{sg} = 90 nm, the capacitances C_{total} = 3.44 aF and C_d = 1.52 aF are extracted from the experimental data in Fig. 3(a) [5] and a series of levels spaced apart by about 7 meV is seen in Fig. 4(a), with a roughly 33-meV gap containing no states in the neighborhood of V_{ds} = 0 V. On the other hand, in the case of the SET with S_{sg} = 140 nm, the capacitances C_{total} = 4.14 aF and C_d = 1.36 aF are extracted from the experimental data in Fig. 3(b) [5], and a series of levels spaced apart by about 5 meV is seen in Fig. 4(b), with a roughly 19-meV gap. However, the series of levels in Fig. 4(b) is less equidistant than that in Fig. 4(a).

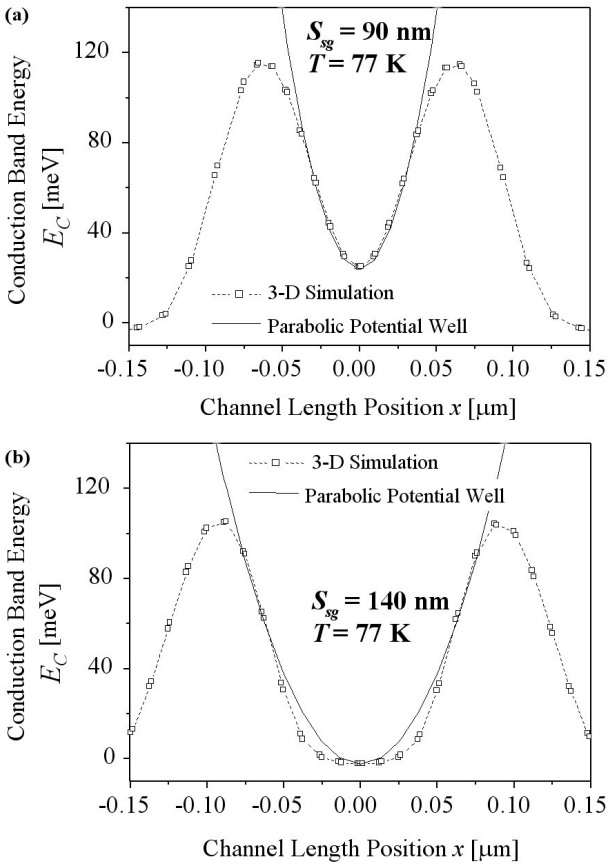

Fig. 5. Comparison of the potential profile calculated by using DAVINCI with the harmonic oscillator approximation: (a) S_{sg} = 90 nm and (b) S_{sg} = 140 nm. The level spacings obtained by using harmonic oscillator approximation, $\hbar\omega_0$, are 6.4 meV, and 3.6 meV, respectively.

To validate the Si QD size dependence of the energy level spacing and its value, we compare the excitation spectrum extracted from experimental results with the 3-D simulation results. Fig. 5 compares the potential profile calculated by using the 3-D device simulator DAVINCI [10] with the harmonic oscillator approximation [11]. The symbols and the solid lines denote the potential shape simulated by using the 3-D device simulator and that obtained approximately with a parabolic potential well, respectively. As Fig. 5 shows, the profile of the electron potential can be approximated by a parabolic confining potential well, *harmonic oscillator*, in the neighborhood of the Fermi level in the Si QD. By the harmonic oscillator approximation, the level spacing is estimated to be 6.4 meV for S_{sg} = 90 nm and 3.6 meV for S_{sg} = 140 nm. The level spaces estimated from the harmonic oscillator approximation at S_{sg} = 90 nm and S_{sg} = 140 nm agree with those extracted from Fig. 3 to within 9 % and 28 %, respectively. Since the harmonic oscillator approximation is based on a 1-dimensional po-

tential well in the length of the SOI wire and does not consider a potential profile in the width of SOI wire, the level spaces estimated from the harmonic oscillator approximation have some errors relative to those extracted from experimental data in Fig 3. Also, since the potential shape in the QD with $S_{sg} = 140$ nm is similar to one mixing a square well with a parabolic well, the level spaces estimated from the harmonic oscillator approximation at $S_{sg} = 140$ nm have larger errors and are less equidistant than those at $S_{sg} = 90$ nm.

IV. CONCLUSIONS

The differential conductance G $(=dI_{ds}/dV_{ds})$ versus V_{ds} data for a gate-induced QD based on a SOI MOSFET were reported. To investigate the transport spectroscopy for a QD in SOI MOSFET, we used two SOI MOSFETs with different sized QDs ($S_{sg} = 90$ nm and 140 nm, respectively), whose tunnel barriers were induced by two sidewall depletion gates on a Si nanowire fabricated on a SIMOX wafer by means of sidewall patterning method. To validate the Si QD size dependence of the energy-level spacing and its value, we compared the excitation spectrum extracted from the experimental data (the differential conductance characteristics) with those calculated from a parabolic confining potential well (harmonic oscillator approximation) approximated from the potential shape simulated by a 3-D device simulator. The energy-level spaces extracted from the experimental data of the sample with $S_{sg} = 90$ nm agree well with those estimated with the harmonic oscillator approximation, but the sample with $S_{sg} = 140$ nm had large errors between the energy-level spaces extracted from the experimental data and those estimated with the harmonic oscillator approximation because the potential shape of the sample with $S_{sg} = 140$ nm was similar to one mixing a square well with a parabolic well.

Considering that recently proposed MOSFET/SET hybrid application schemes based on Si SETs [6,12–16] are more complex and more sophisticated and that the quantum effects become more pronounced as the size of Si QD decreases for the purpose of room-temperature operation, more attention should be paid to the excited quantum state of a Si QD in designing the Si QD-based system. In these viewpoints, our result shows that a parabolic confining potential well is a useful guide in scaling down and optimizing a Si QD, in that the single-particle states can be simply estimated from the harmonic oscillator approximation.

ACKNOWLEDGMENTS

This work was supported by research program 2006 of Kookmin University in Korea, and the CAD software was supported by the IC Design Education Center (IDEC).

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