Journal of the Korean Physical Society, Vol. 58, No. 5, May 2011, pp. 1518∼1521

Study on the Oxide Trap Distribution in a Thin Gate Oxide from Random Telegraph Noise in the Drain Current and the Gate Leakage Current

Heung-Jae Cho,* Younghwan Son, Sanghoon Lee, Jong-Ho Lee, Byung-Gook Park and Hyungcheol Shin
School of Electrical Engineering and Computer Science, Seoul National University, Seoul 151-742, Korea

(Received 11 July 2010)

Random telegraph noise in the drain current (I_d RTN) and the gate current (I_g RTN) has been studied to characterize slow oxide traps in a thin gate oxide. First, I_g RTN was classified into two categories from its dependence on gate bias. Through the analysis of I_d and I_g RTNs, the distribution of oxide traps in the thin oxide was also studied. Most of the oxide traps obtained from I_d RTN were found to be in the middle range of the oxide and to have an energy level within a narrow range whereas the oxide traps from I_g RTN were widely distributed.

PACS numbers: 68.35.-p
Keywords: RTN, I_g RTN, I_d RTN, Oxide trap distribution, Trap location, Trap energy level
DOI: 10.3938/jkps.58.1518

I. INTRODUCTION

As devices continue to scale down in MOSFET technology, low-frequency noise becomes more and more important in determining MOSFET performance. Especially, the low-frequency noise of small MOSFET devices is dominated by random telegraph noise in the drain current (I_d RTN). Therefore, considerable research on the I_d RTN has been performed [1–7]. Recently, the gate oxide thickness has been getting thinner with scaling device size, and the gate leakage current has increased due to direct tunneling through the thin gate oxide. Since the transport of a high gate leakage current is affected by oxide properties, some studies on the transport have been conducted in order to characterize ultra-thin gate oxides or high-k gate dielectrics. One of these efforts is the low-frequency noise measurement of the gate leakage current in MOSFET devices. The low-frequency noise measurement is reported to be an effective way to extract the effective trap density inside the gate dielectrics [8,9]. In addition, random telegraph noise in the gate leakage current (I_g RTN) has also been observed in small devices when a slow oxide trap is located in the gate dielectric and reported to be sensitive to slow oxide traps in the gate dielectric [10–14]. Furthermore, the combined technique of both I_d and I_g RTNs has been introduced to analyze slow oxide traps [12]. However, there is no report on the distribution of slow oxide traps in the gate oxide by using the technique.

In this work, we studied slow oxide traps in a thin gate oxide by using I_d and I_g RTNs. Two kinds of I_g RTNs as functions of the gate bias were introduced. Then methods for extracting the location and the energy level of an oxide trap by using the bias dependency are discussed. Finally, we characterized the distribution of oxide trap in the thin gate oxide through an analysis of the vertical location and the energy level of oxide traps extracted from both the I_d and the I_g RTN.

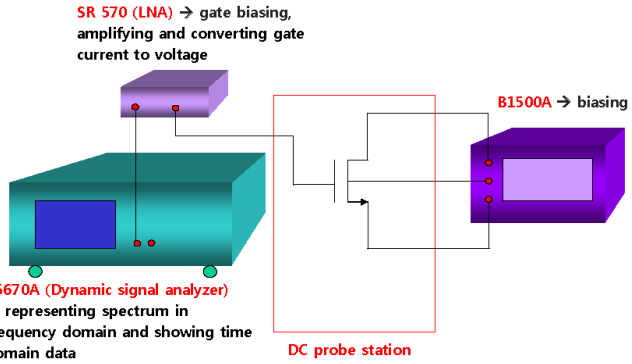

Fig. 1. (Color online) Low-frequency noise measurement system.

II. EXPERIMENT AND DISCUSSION

The N+poly-Si gated nMOSFETs were fabricated on p-type Si (100) substrates by using standard 80 nm DRAM technology. The gate oxide thickness was 2.6 nm. The tested devices had channel width of 7.25 um and channel length of 0.13 um. Figure 1 shows the low-frequency noise measurement system to measure the

*E-mail: hjaecho7@snu.ac.kr; Fax: +82-2-882-4658

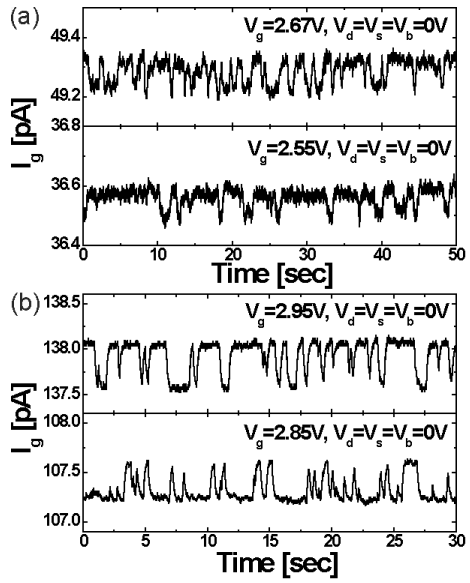

Fig. 2. Two kinds of I_g RTN. (a) Type A shows that τ_c and τ_e decreases and slightly increases, respectively, with respect to V_{gs}. (b) Type B shows that τ_c and τ_e increases and decreases, respectively.

RTN. The SR 570 low noise amplifier (LNA) amplifies the gate leakage current and converts it to a voltage, then an HP35670A dynamic signal analyzer shows the low-frequency noise behavior both in the time and in the frequency domains. To reduce external noise, the SR 570 LNA is operated by using a battery, and the device is shielded by using a shielding box. Slow oxide traps obtained from I_d RTN were observed within the gate voltage (V_{gs}) range of 0.7 ∼ 1.2 V with the drain voltage (V_{ds}) at 50 mV while the traps from I_g RTN were measured within the V_{gs} range of 2.5 ∼ 3.8 V.

The I_g RTN phenomenon was reproductively found in ∼3% of samples from several nMOSFET devices (more than 400 ea). Two kinds of I_g RTNs were also observed. In one group (Type A) of devices, the time constant for a high current level decreases and that for a low current level slightly increases with increasing V_{gs}, as shown in Fig. 2(a), whereas in the other group (Type B), the opposite tendency is observed, as shown in Fig. 2(b). These figures show two discrete current levels, meaning that there is a single oxide trap in the gate oxide. The times for the high and the low current levels are assumed to be the capture time (τ_c) and the emission time (τ_e), respectively, because each electron trapped in the oxide during τ_e blocks the current conduction through the gate oxide [15]. The capture and the emission time constants with respect to V_{gs} ($d\ln(\tau_c/\tau_e)/dV_g$) were analyzed to characterize the oxide trap, as shown in Fig. 3. Type A shows a negative slope in $d\ln(\tau_c/\tau_e)/dV_g$ whereas Type B shows a positive slope. These can be explained that Type A interacts with the Si channel due to the increase in the probability of trap occupation with increasing V_{gs} [1–6, 10–13] while Type B interacts with the gate electrode

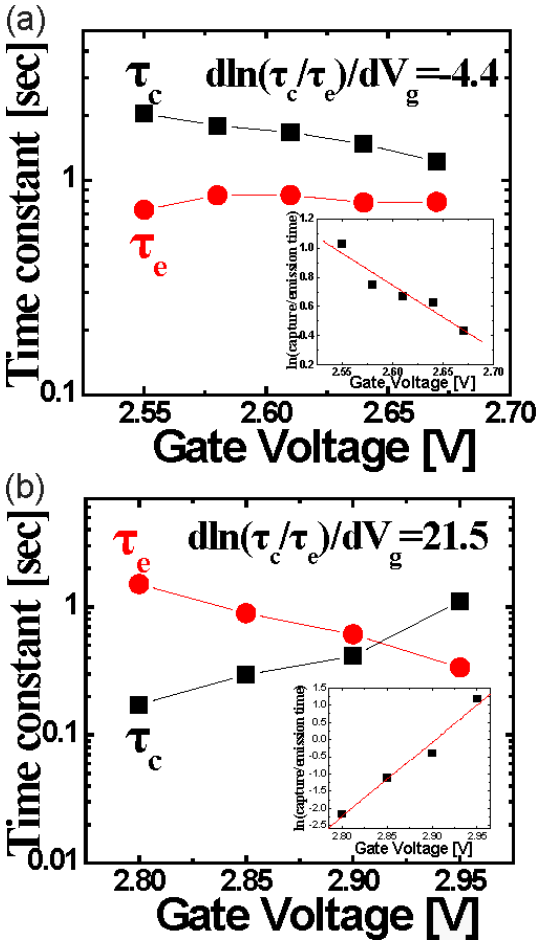

Fig. 3. (Color online) Average capture and emission time constants as functions of V_{gs}. Type A (a) shows a negative slope in $d\ln(\tau_c/\tau_e)/dV_g$ whereas Type B (b) shows a positive slope. The inset is the time-constant variation rate with respect to V_{gs}.

due to the decrease in the probability of trap occupation [11,13,14]. For Type A, the energy level and the vertical location of an oxide trap can be extracted from the conventional equation based on the grand partition function [1–3,5,6]

$$\ln\frac{\tau_c}{\tau_e} = \frac{1}{k_BT}\Big[(E_{Cox}-E_T)+q\frac{x_T}{T_{ox}}V_{ox} - (E_C-E_{Fp}+qV_C)-q\phi_0+q\psi_s\Big],$$

where

$$V_{ox}=V_{gs}-V_{FB}-\psi_p-\psi_s. \quad (1)$$

Here, k_B is the Boltzmann constant, T is the absolute temperature, E_{Cox} is the conduction band edge of the oxide, E_T is trap energy level, E_C is the conduction band edge of the Si, and E_{Fp} is hole Fermi level. V_c is the channel potential at a point y in the channel measured from the source ($V_c = yV_{ds}/L$ at low drain voltage), Φ_0

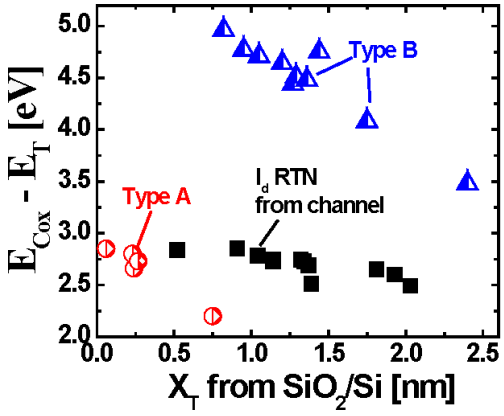

Fig. 4. (Color online) Distribution of slow oxide traps as a function of trap's vertical location in the gate oxide. Type A represents oxide traps interacting with the Si channel whereas Type B corresponds to oxide traps interacting with the gate electrode.

is the difference between the conduction bands of Si and SiO_2, ψ_s is the amount of surface band-bending, ψ_p is the amount of band-bending in the poly-Si gate, V_{ox} is the oxide voltage drop, T_{ox} is oxide physical thickness, and x_T is the position of the trap in the gate oxide from the SiO_2/Si interface. In the equation above, the Fermi level for electrons (E_{Fn}) is written in terms of E_{Fp} and V_c: $E_{Fn} = E_{Fp}$ - qV_c.

In the opposite case (Type B), the vertical location and the energy level of the oxide trap can be extracted from [14]

$$\ln\frac{\tau_c}{\tau_e} = \frac{1}{k_BT}\left[(E_{Cox}-E_T)+q\frac{(T_{ox}-x_{TGate})}{T_{ox}}V_{ox} - q\left(\phi_0+V_{ox}+\psi_p\right)\right]. \quad (2)$$

Here, x_{TGate} is the position of the trap in the gate oxide from poly-Si/SiO_2 interface.

Through an analysis of the two kinds of I_g RTNs, we observed the distribution of slow oxide traps, as shown in Figs. 4 and 5. In these plots, slow oxide traps extracted from I_d RTN are also displayed to compare to those obtained from the I_g RTN. Slow oxide traps obtained from I_d RTN were observed within the V_{gs} range of 0.7 $\sim$ 1.2 V while the traps from I_g RTN were separately measured within the V_{gs} range of 2.5 $\sim$ 3.8 V. The reason for the apparent absence of I_g RTN in the lower V_{gs} range is that I_g is small enough to be negligible whereas the absense of I_d RTN in the higher V_{gs} range is related to the trap-potential screening effect caused by a high inversion carrier concentration [1,2].

Most of the oxide traps obtained from I_d RTN were found to be located in the middle of the oxide. The slow oxide traps in Type A were observed to exist near the SiO_2/Si interface and to have an energy level range (2.2 $\sim$ 2.9 eV) similar to that of the oxide traps from I_d RTN while the oxide traps in Type B were distributed from

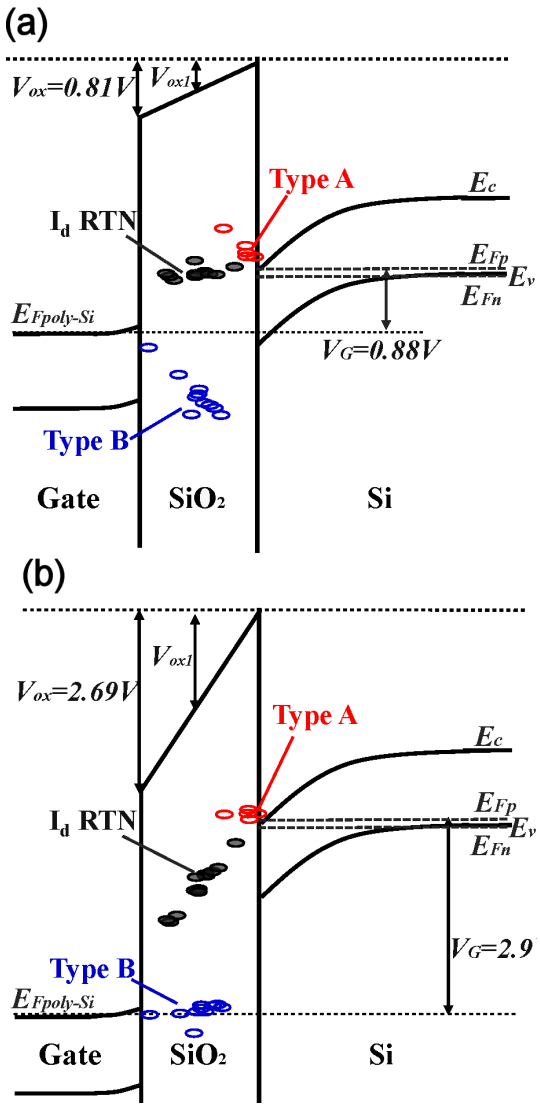

Fig. 5. (Color online) Distribution of slow oxide traps in energy band diagrams at a (a) V_{gs} of 0.88 V with a V_{ds} of 50 mV and a (b) V_{gs} of 2.9 V with a V_{ds} of 50 mV. Here, V_{ox1} is the voltage drop at a trap in SiO_2.

the middle of oxide to the poly-Si/SiO_2 interface and had a relatively deep energy level range of 3.5 $\sim$ 4.96 eV. The reason for the discrete observations as I_d RTN or I_g RTN (Type A) for oxide traps that have similar energy levels can be explained by the geometric effect of the oxide traps in the gate oxide, as shown in Fig. 5. The oxide traps observed in I_d RTN and I_g RTN (Type A) exist at energies above the E_{Fn} of Si at low V_{gs} due to their low energy level. With increasing V_{gs}, the oxide traps move down to the E_{Fn} through the increase of V_{ox1}, which is the voltage drop at a trap in SiO_2, and interact with the Si channel because the random trapping/detrapping process of carriers in an oxide takes place when the trap energy level is aligned to E_{Fn} within a range of a few k_BT. This indicates that the magnitude of V_{ox1}

with respect to V_{gs} depends on the trap position in the gate oxide. The closer to the SiO_2/Si interface that an oxide trap is located, the less the amount of V_{ox1} change in the energy-band diagram. In other words, more V_{gs} is needed to move down the trap energy level to E_{Fn} in the channel. At a low V_{gs} of 0.88 V in Fig. 5(a), the oxide traps from I_d RTN become close to the E_{Fn} in the Si channel while the Type A oxide traps are still located far above the E_{Fn}, indicating that the Type A oxide traps are not active at the V_{gs}. However, at a high V_{gs} of 2.9 V, as shown in Fig. 5(b), the oxide traps from I_d RTN move much below the E_{Fn} whereas the Type A oxide traps become close to the E_{Fn} and interact with the Si channel.

Figure 5 also shows the distribution of Type B oxide traps. We observed that the Type B oxide traps were more frequently measured and that their distribution was wider than that of the Type A oxide traps. The reason may be due to their deep energy levels and different dependences on V_{gs}. With increasing V_{gs}, the Type A oxide traps move down toward E_{Fn} whereas the Type B oxide traps move upward $E_{Fpoly-Si}$ and interact with the gate electrode. Thus, the slow oxide traps below $E_{Fpoly-Si}$ can only be detected by the I_g RTN measurements whereas the oxide traps above the E_{Fn} of Si can be measured by using both I_d RTN and I_g RTN, as shown in Fig. 5. These results indicate that an I_g RTN analysis is complementary to that of I_d RTN and provides additional insight in order to characterize slow oxide traps in a thin gate oxide.

III. CONCLUSION

We studied slow oxide traps in a thin gate oxide and found two kinds of I_g RTNs from their dependences on the gate bias. Through an analysis of the trap's vertical location and energy level extracted from I_g RTN and I_d RTN, the distribution of slow oxide traps in the thin gate oxide was also studied. Most of the oxide traps obtained from I_d RTN were found to be in the middle range of the oxide and to have an energy level within a narrow range. On the other hand, oxide traps from the two kinds of I_g RTNs were widely distributed.

ACKNOWLEDGMENTS

This work is supported in part by the Hynix Semiconductor Incorporation and in part by the Inter-university Semiconductor Research Center (ISRC).

REFERENCES

[1] M. J. Kirton and M. J. Uren, Adv. Phys. **38**, 367 (1989).
[2] K. K. Hung, P. K. Ko, C. Hu and Y. C. Cheng, IEEE Electron Device Lett. **11**, 90 (1990).
[3] H. Lee, Y. Yoon, S. Cho and H. Shin, IEICE Trans. Electron. **E90-C**, 968 (2007).
[4] Z. Celik-Butler, P. Vasina and N. V. Amarasinghe, IEEE Trans. Electron Devices **47**, 646 (2000).
[5] S. Yang, H. Lee and H. Shin, Jpn. J. Appl. Phys. **47**, 2606 (2008).
[6] S. Yang, K. H. Yeo, D.-W. Kim, K.-I. Seo, D. Park, G. Jin, K. Oh and H. Shin, IEDM Tech. Dig., 765 (2008).
[7] J.-H. Lee, S.-Y. Kim, I. Cho, S. Hwang and J.-H. Lee, J. Semicond. Technol. Sci. **6**, 38 (2006).
[8] P. Magnone, C. Crupi, G. Iannaccone, G. Giusi, C. Pace, E. Simoen and C. Claeys, in *Proceeding 9th International Conference on Ultimate Integration of Silicon* (Udine, Italy, March 12-14, 2008), p. 141.
[9] P. Magnone, L. Pantisano, F. Crupi, L. Trojman, C. Pace and G. Giusi, IEEE Electron Device Lett. **29**, 1056 (2008).
[10] F. Martinez, C. Leyris, G. Neau, M. Valenza, A. Hoffmann, J. C. Vildeuil, E. Vincent, F. Boeuf, T. Skotnicki, M. Bidaud, D. Barge and B. Tavel, Miroelectron. Eng. **80**, 54 (2005).
[11] C. M. Chang, S. S. Chung, Y. S. Hsieh, L. W. Cheng, C. T. Tsai, G. H. Ma, S. C. Chien and S. W. Sun, IEDM Tech. Dig., 787 (2008).
[12] L. Zhang, J. Zhuge, R. Wang, R. Huang, C. Liu, D. Wu, Z. Kang, D.-W. Kim, D. Park and Y. Wang, VLSI Technol. Syst., 46 (2009).
[13] S. Lee, H.-J. Cho, Y. Son, D. S. Lee and H. Shin, IEDM Tech. Dig., 763 (2009).
[14] H.-J. Cho, S. Lee, B.-G. Park and H. Shin, Solid. State Electron. **54**, 362 (2010).
[15] H.-J. Cho, Y. Son, B.-C Oh, S. Lee, J.-H Lee, B.-G. Park and H. Shin, IEEE Electron Device Lett. **31**, 1029 (2010).